√Form 1449 (Modified)	Atty Docket No.	Application No.:
	ALTRP061	09/783,246
Information Disclosure Statement By Applicant	Applicant: Hutton	
	Filing Date	Group
(Use Several Sheets if Necessary)	2/13/01	2644

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
MCH	A1	5,550,782	8/27/96	Cliff et al.			5/18/94
MCH	A2	5,689,195	11/18/97	Cliff et al.			5/17/95
MCH	A3	6,215,326	4/10/01	Jefferson et al.			3/10/99
MCH	A4	5,659,484	8/19/97	Bennett et al.			

Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation Yes	Translation No

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
MCH	B1	Hutton et al., "Timing-Driven Placement for Hierarchical Programmable Logic Devices". Talk describing aspects of the invention. Monterey, California –February 11, 2001 (paper attached).
MCH	B2	V. Betz, Architecture and CAD for Speed and Area Optimization of FPGA's", Ph.D. Dissertation, University of Toronto, 1998.
MCH	B3	Jason Cong et al., "Large Scale Circuit Partitioning with Loose/Stable Net Removal and Signal Flow Based Clustering", Proc. IEEE Int'l Conference on Computer-Aided Design, pp. 441-446, November 1997.
MCH	B4	W.E. Donath et al., "Timing Driven Placement Using Complete Path Delays", in Proc. 27th ACM/IEEE Design Automation Conference, pp.84-89, 1990.
MCH	B5	Carl Ebeling et al., "Placement and Routing Tools for theTriptych FPGA", IEEE Trans. On VLSI, Vol. 3, No. 4, pp. 473-481, December 1995.
MCH	B6	Jon Frankle, "Iterative and Adaptive Slack Allocation for Performance-Driven Layout and FPGE Routing", in Proc. 29th ACM/IEEE Design Automation Conference, pp 536-542, 1992.

Examiner	Date Considered
Mary C. Hogan	7/27/04

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

BEST AVAILABLE COPY

Form 1449 (Modified)	Atty Docket No.	Application No.:
	ALTRP061	09/783,246
Information Disclosure Statement By Applicant	Applicant: Hutton	
	Filing Date	Group
(Use Several Sheets if Necessary)	2/13/01	2644

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
MCH	B7	P. Leventis, "Placement algorithms and routing architecture for long-line based FPGA's", Bachelor thesis, University of Toronto 1999.
MCH	B8	Alexander Marquardt et al., "Timing-Driven Placement for FPGA's", in Proc. ACM/SIGDA FPGA Conference, FPGA00, pp. 203-213, 2000.
MCH	B9	Sudip K. Nag and Rob A. Rutenbar, "Performance-Driven Simultaneous Placement and Routing for FPGA's". IEEE Trans. On CAD for Integrated Circuits and Systems, Vol. 17, No. 6, pp. 499-518, June 1998.
MCH	B10	Shih-Lian Ou and Massoud Pedram, "Timing-Driven Placement Based on Partitioning with Dynamic Cut-net Control", in Proc. 37th ACM/IEEE Design Automation Conference, pp. 472-476, 2000.
MCH	B11	Laura A. Sanchis, "Multiple-way network partitioning", IEEE Trans. On Computers, Vol. 38, No. 1, January 1989.
MCH	B12	Prashant Sawkar and Donald Thomas, "Multi-Way Partitioning for Minimum Delay for Look-Up Table Based FPGAs". In Proc. 32nd ACM/IEEE Design Automation Conference, pp. 201-205, 1995.
MCH	B13	S.A. Senouci et al., "Timing-Driven Floorplanning on Programmable Hierarchical Targets", in Proc. ACM/SIGDA FPGA Conference, FPGA98, pp. 85-92, 1998.
MCH	B14	S. Sutanthavibul and E. Shragowitz, "Dynamic Prediction of Critical Paths and Nets for Constructive Timing-Driven Placement", in Proc. 28th ACM/IEEE Design Automation Conference, pp. 632-635, 1991.
MCH	B15	W. Swartz and C. Sechen, "Timing-Driven Placement for Large Standard Cell Circuits", in Proc. 32nd ACM/IEEE Design Automation Conference, pp. 211-215, 1995.

Examiner	Mary C. Hogan	Date Considered	7/27/04

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.